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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/730,120	SHIBATA, KOHSAKU	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to the Applicant's Response mailed on December 15, 2006. Claims 1-23 were amended. Claims 1-23 of the application are pending. This office action is made final.

Substitute Specification

2. The substitute specification mailed on December 15, 2006 has been accepted and entered.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-21 use the words, "operable to" or are dependent on claims that use these words. The use of the words "operable to" make the claims indefinite since they state what the claims are capable of doing but do not state what the claims actually do.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1, 2, 5, 6, 8, 9, 22 and 23 are rejected under 35 U.S.C. § 102(e) as being anticipated by **Moller et al.** (U.S. Patent 6,826,522).

6.1 **Moller et al.** teaches method and apparatus for improved efficiency in pipeline simulation and emulation. Specifically, as per claim 1, **Moller et al.** teaches a simulation apparatus for simulating a very long instruction word processor (Abstract, L14-16; CL1, L20-22; CL2, L13-14; CL4, L29-37; CL4, L47-49; Fig. 1); the simulation apparatus comprising:

a first simulation unit operable to simulate execution of a group of instructions intended to be simultaneously executed, and to generate a first simulation result (Fig. 4: shows a group of instructions executed on a cycle e.g. cycle 5 with instructions I2-I5; Fig. 8; Fig. 13; CL1, L35-38; CL1, 51-54; CL6, L31-34; CL4, L29-37; CL4, L47-49; Fig. 1; CL6, L37-40; CL8, 21-23; CL8, L55-57) ; and

a second simulation unit operable to simulate, based on the first simulation result generated by the first simulation unit, a sequential execution of the group of instructions on an instruction-by-instruction basis and to generate a second simulation result (CL1, L29-33; Fig. 6: Shows one instruction I1 in one cycle; CL2, L17-30; CL6, L46-51; CL6, L56-62; CL8, L63-65).

Per claim 2: **Moller et al.** teaches the second simulation unit is operable to generate the second simulation result by undoing the simulation of the execution of one of the instructions from the group of instructions previously simulated by the first simulation unit (CL1, L29-33; Fig. 6: Shows one instruction I1 in one cycle; CL2, L17-30; CL6, L46-51; CL6, L56-62; CL8, L63-65).

Per claim 5: **Moller et al.** teaches the first simulation unit is operable to simulate a pipeline processor that simultaneously executes a plurality of instructions (CL1, L41-59; Abstract, L2-3 and L6-16; Fig. 4; CL1, L20-22; CL1, L51-59; CL6, L31-34); and

the simulation apparatus further comprises a display image generation unit operable to generate a display image showing instructions included in a pipeline based on the first simulation results generated by the first simulation unit and the second simulation results generated by the second simulation unit (Fig. 4; CL6, L35-41; Fig. 6).

Per claim 6: **Moller et al.** teaches that the display image contains a representation of an instruction included in every stage of the pipeline (Fig. 4; CL6, L35-41; Fig. 6).

Per claims 8 and 9: **Moller et al.** teaches that the display image contains a representation of each instruction included in the pipeline; and the display image contains a representation of each instruction included in every stage of the pipeline (Fig. 4; CL6, L35-41).

6.2 As per Claims 22 and 23, these are rejected based on the same reasoning as Claim 1, supra. Claims 22 and 23 are simulation method and computer-readable recording medium claims reciting the same limitations as Claim 1, as taught throughout by **Moller et al.**

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 3-4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Moller et al.** (U.S. Patent 6,826,522) in view of **Matsumoto et al.** (U.S. Patent Application 2003/0204819).

9.1 As per claim 3, **Moller et al.** teaches the simulation apparatus of claim 1. **Moller et al.** does not expressly teach a display control unit operable to control a display unit to display the second simulation result generated by the second simulation unit. **Matsumoto et al.** teaches a display control unit operable to control a display unit to display the second simulation result generated by the second simulation unit (Page 5, Para 0104, L1-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the simulation apparatus of **Moller et al.** with the simulation apparatus of **Matsumoto et al.** that included a display control unit operable to control a display unit to display the second simulation result generated by the second simulation unit, because that would allow outputting the execution result of debug command when a specific address is passed; outputting an error, when an error has occurred; outputting intermediate results on the display terminal, so the user could check if the simulation was progressing as expected and the device was executing normally (Page 5, Para 0104, L1-13).

9.2 As per claim 4, **Moller et al.** teaches the simulation apparatus of claim 2. **Moller et al.** does not expressly teach that the second simulation unit includes a judgment unit operable to judge whether or not an instruction that satisfies a break condition is included in the execution of the group of instructions previously simulated by the first simulation unit; an indication unit

operable to direct the first simulation unit to simulate execution of a next group of instructions when the judgment unit judges that no instruction satisfying the break condition is included in the execution of the group of instructions previously simulated by the first simulation unit; a determination unit operable to determine that an instruction of the group of instructions is a stop instruction when the judgment unit judges that the instruction satisfying the break condition is included; and a generation unit operable to generate a simulation result by undoing simulations of the execution of the stop instruction and subsequent instructions in the execution of the group of instructions previously simulated. **Matsumoto et al.** teaches that the second simulation unit includes a judgment unit operable to judge whether or not an instruction that satisfies a break condition is included in the execution of the group of instructions previously simulated by the first simulation unit (Page 5, Para 0104, L1-9); an indication unit operable to direct the first simulation unit to simulate execution of a next group of instructions when the judgment unit judges that no instruction satisfying the break condition is included in the execution of the group of instructions previously simulated by the first simulation unit (Page 5, Para 0104, L1-9); a determination unit operable to determine that an instruction of the group of instructions is a stop instruction when the judgment unit judges that the instruction satisfying the break condition is included (Page 5, Para 0104, L1-9); and a generation unit operable to generate a simulation result by undoing simulations of the execution of the stop instruction and subsequent instructions in the execution of the group of instructions previously simulated (Page 5, Para 0104, L1-9; Para 0108, L16-18).

9.3 As per claim 7, **Moller et al.** teaches the simulation apparatus of claim 1. **Moller et al.** teaches that the first simulation unit is operable to simulate, on a cycle-by-cycle basis, a pipeline processor that simultaneously executes a plurality of instructions (Abstract, L2-3 and L6-16; Fig. 4; CL1, L20-22; CL1, L51-59; CL6, L31-34).

Moller et al. does not expressly teach an acception unit operable to accept a user instruction for indicating a step to be executed on the instruction-by-instruction basis and for indicating a step to be executed on the cycle-by-cycle basis; and a display image generation unit operable to generate a display image showing the second simulation result generated by the second simulation unit when the user instruction that indicates the step to be executed on the instruction-by-instruction basis is accepted by the acception unit, and to generate a display image showing a simulation result generated on the cycle-by-cycle basis by the first simulation unit when the user instruction that indicates the step to be executed on the cycle-by-cycle basis is accepted by the acception unit.

Matsumoto et al. teaches that an acception unit operable to accept a user instruction for indicating a step to be executed on the instruction-by-instruction basis and for indicating a step to be executed on the cycle-by-cycle basis (Page 7, Para 0128, L2-5; Para 0129); and a display image generation unit operable to generate a display image showing the second simulation result generated by the second simulation unit when the user instruction that indicates the step to be executed on the instruction-by-instruction basis is accepted by the acception unit (Page 5, Para 0104, L1-3), and to generate a display image showing a simulation result generated on the cycle-by-cycle basis by the first simulation unit when the user instruction that indicates the step

to be executed on the cycle-by-cycle basis is accepted by the acception unit (Page 5, Para 0104, L1-3).

10. Claims 10-18 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Moller et al.** (U.S. Patent 6,826,522) in view of **Matsumoto et al.** (U.S. Patent Application 2003/0204819), and further in view of **Ussery et al.** (U.S. Patent Application 2001/0025363).

10.1 As per claim 10, **Moller et al.** teaches the simulation apparatus of claim 1. **Moller et al.** teaches a first simulator operable to update the first data by simulating an execution of a single group of instructions after the storage unit stores the copy of the first data (Abstract, L2-3 and L6-16; Fig. 4; CL1, L20-22; CL1, L51-59; CL6, L31-34). **Moller et al.** teaches that the second simulation unit is operable to obtain the second simulation results of the execution of the group of instructions on the instruction-by-instruction basis based on the first data and the second data (CL6, L44-62; Fig. 5 and Fig. 6; CL8, L65-66).

Moller et al. does not expressly teach that the first simulation unit includes a hold unit operable to hold first data indicating resources of the very long instruction word processor. **Matsumoto et al.** teaches that the first simulation unit includes a hold unit operable to hold first data indicating resources of the very long instruction word processor (Page 7, Para 0129; Page 8, Para 0159 and Para 0160; Page 13, Para 0315 and Para 0324; Page 14, Para 0336). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the simulation apparatus of **Moller et al.** with the simulation apparatus of **Matsumoto et al.** that

included the first simulation unit including a hold unit operable to hold first data indicating resources of the very long instruction word processor, because that would allow identifying the slot position of the instruction in the VLIW mode (simultaneous operation) and the register resources used (Page 8, Para 0159 and 0160; Page 7, Para 0129); and proper delay between instructions stages could be allowed if a register was write accessed first and immediately after that it was read-accessed, so the instructions executed successfully (Page 13, Para 0315, 0321 and 9324).

Moller et al. and **Matsumoto et al.** do not expressly teach that the first simulation unit includes a storage unit operable to store a copy of the first data in the memory unit as second data. **Ussery et al.** teaches that the first simulation unit includes a storage unit operable to store a copy of the first data in the memory unit as second data (Page 2, Para 0015 and Para 0022). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the simulation apparatus of **Moller et al.** and **Matsumoto et al.** with the simulation apparatus of **Ussery et al.** that included the first simulation unit including a storage unit operable to store a copy of the first data in the memory unit as second data, because that would allow design of the VLIW architectures by varying the location of the processors and the memory units in the data path and evaluating the effects of locations on VLIW processor performance by simulation (Page 1, Para 0012, L3-6; Para 0013, L1-8; Fig. 1, Items 116 and 119).

10.2 As per claim 11, **Moller et al., Matsumoto et al.** and **Ussery et al.** teach simulation apparatus of claim 10. **Moller et al.** teaches that the second simulation unit is operable to

reconstruct data indicating a resource of the very long instruction word processor before executing the simulation of the instruction of the group of instructions on the instruction-by-instruction basis (CL6, L44-62; Fig. 5 and Fig. 6; CL8, L65-66).

Moller et al. and **Matsumoto et al.** do not expressly teach that the storage unit is operable to store register data in the memory unit as the second data. **Ussery et al.** teaches that the storage unit is operable to store register data in the memory unit as the second data (Page 2, Para 0015 and Para 0022).

10.3 As per claim 12, **Moller et al., Matsumoto et al.** and **Ussery et al.** teach simulation apparatus of claim 11. **Moller et al.** and **Matsumoto et al.** do not expressly teach that the storage unit is operable to store memory data before memory writing, in the hold unit, and to store the memory data so that the memory data is contained in the second data when a memory write instruction is included in the group of instructions. **Ussery et al.** teaches that the storage unit is operable to store memory data before memory writing, in the hold unit, and to store the memory data so that the memory data is contained in the second data when a memory write instruction is included in the group of instructions (Page 2, Para 0015 and Para 0022).

10.4 As per claim 13, **Moller et al., Matsumoto et al.** and **Ussery et al.** teach simulation apparatus of claim 10. **Moller et al.** does not expressly teach that the second simulation unit includes a judgment unit operable to judge whether or not an instruction that satisfies a break condition is included in the execution of the group of instructions previously simulated by the first simulation unit; an indication unit operable to direct the first simulation unit to simulate

execution of a next group of instructions when the judgment unit judges that no instruction satisfying the break condition is included in the execution of the group of instructions previously simulated by the first simulation unit; a determination unit operable to determine that an instruction is a stop instruction when the judgment unit judges that the instruction satisfying the break condition is included. **Matsumoto et al.** teaches that the second simulation unit includes a judgment unit operable to judge whether or not an instruction that satisfies a break condition is included in the execution of the group of instructions previously simulated by the first simulation unit (Page 5, Para 0104, L1-9); an indication unit operable to direct the first simulation unit to simulate execution of a next group of instructions when the judgment unit judges that no instruction satisfying the break condition is included in the execution of the group of instructions previously simulated by the first simulation unit (Page 5, Para 0104, L1-9); and a determination unit operable to determine that an instruction is a stop instruction when the judgment unit judges that the instruction satisfying the break condition is included (Page 5, Para 0104, L1-9).

10.5 As per claim 14, **Moller et al., Matsumoto et al.** and **Ussery et al.** teach simulation apparatus of claim 13. **Moller et al.** does not expressly teach that the determination unit is operable to determine that an instruction next to a present stop instruction is a break condition in a step of execution of a simulation performed on an instruction-by-instruction basis. **Matsumoto et al.** teaches that the determination unit is operable to determine that an instruction next to a present stop instruction is a break condition in a step of execution of a simulation performed on an instruction-by-instruction basis (Page 5, Para 0104, L1-9).

10.6 As per claim 15, **Moller et al., Matsumoto et al.** and **Ussery et al.** teach simulation apparatus of claim 13. **Moller et al.** does not expressly teach that the second simulation unit further comprises a reconstruction unit operable to reconstruct, based on the first data and the second data, data indicating the resources of the very long instruction word processor, on a condition that execution of previous instructions, up to an instruction just prior to the stop instruction determined by the determination unit, has been simulated. **Matsumoto et al.** teaches that the second simulation unit further comprises a reconstruction unit operable to reconstruct, based on the first data and the second data, data indicating the resources of the very long instruction word processor (Page 7, Para 0129; Page 8, Para 0159 and Para 0160; Page 13, Para 0315 and Para 0324; Page 14, Para 0336), on a condition that execution of previous instructions, up to an instruction just prior to the stop instruction determined by the determination unit, has been simulated (Page 5, Para 0104, L1-9).

10.7 As per claim 16, **Moller et al., Matsumoto et al.** and **Ussery et al.** teach simulation apparatus of claim 13. **Moller et al.** does not expressly teach that the second simulation unit further comprises a reconstruction unit operable to reconstruct, based on the first data and the second data, data indicating the resources of the very long instruction word processor, on a condition that execution of previous instructions, up to the stop instruction determined by the determination unit, has been simulated. **Matsumoto et al.** teaches that the second simulation unit further comprises a reconstruction unit operable to reconstruct, based on the first data and the second data, data indicating the resources of the very long instruction word processor, on a condition that execution of previous instructions, up to the stop instruction determined by the

determination unit, has been simulated (Page 7, Para 0129; Page 8, Para 0159 and Para 0160; Page 13, Para 0315 and Para 0324; Page 14, Para 0336).

10.8 As per claim 17, **Moller et al., Matsumoto et al.** and **Ussery et al.** teach simulation apparatus of claim 16. **Moller et al.** does not expressly teach that the first simulator is operable to generate update information indicating resources of the very long instruction word processor to be changed by each instruction of the group of instructions, and the reconstruction unit is operable to reconstruct the data from the resources of the very long instruction word processor that correspond to a result of a sequential execution of the instructions of the group of instructions according to the first data, the second data, and the update information. **Matsumoto et al.** teaches that the first simulator is operable to generate update information indicating resources of the very long instruction word processor to be changed by each instruction of the group of instructions (Page 7, Para 0129; Page 8, Para 0159 and Para 0160; Page 13, Para 0315 and Para 0324; Page 14, Para 0336), and the reconstruction unit is operable to reconstruct the data from the resources of the very long instruction word processor that correspond to a result of a sequential execution of the instructions of the group of instructions according to the first data, the second data, and the update information (Page 7, Para 0129; Page 8, Para 0159 and Para 0160; Page 13, Para 0315 and Para 0324; Page 14, Para 0336).

10.9 As per claim 18, **Moller et al., Matsumoto et al.** and **Ussery et al.** teach simulation apparatus of claim 10. **Moller et al.** teaches that the first simulator is operable to simulate an execution of the group of instructions on a cycle-by-cycle basis of pipeline processing (Abstract,

L2-3 and L6-16; Fig. 4; CL1, L20-22; CL1, L51-59; CL6, L31-34), and the simulation apparatus is operable to count a quantity of execution cycles in the simulation for every group of instructions (Fig. 4; CL6, L35-41).

10.10 As per claim 20, **Moller et al., Matsumoto et al.** and **Ussery et al.** teach simulation apparatus of claim 18. **Moller et al.** does not expressly teach that the first simulator is operable to simulate a delay cycle according to a delay instruction that causes a delay cycle in an execution stage of the very long instruction word processor to be simulated; and the reconstruction unit is operable to reconstruct data indicating the resources of the very long instruction word processor that correspond to a simulation result from simulating the delay cycle according to update information for the delay instruction. **Matsumoto et al.** teaches that the first simulator is operable to simulate a delay cycle according to a delay instruction that causes a delay cycle in an execution stage of the very long instruction word processor to be simulated (Page 13, Para 0321 and Para 0324; Fig. 28), and the reconstruction unit is operable to reconstruct data indicating the resources of the very long instruction word processor that correspond to a simulation result from simulating the delay cycle according to update information for the delay instruction (Page 7, Para 0129; Page 8, Para 0159 and Para 0160; Page 13, Para 0315 and Para 0324; Page 14, Para 0336).

10.11 As per claim 21, **Moller et al., Matsumoto et al.** and **Ussery et al.** teach simulation apparatus of claim 20. **Moller et al.** does not expressly teach that the reconstruction unit is operable to generate data indicating the resources of the very long instruction word processor

that correspond to a simulation result of simulating an output dependency instruction according to the update information for the delay instruction and according to the update information for the output dependency instruction that has an output dependency in the same group of instructions as the delay instruction. **Matsumoto et al.** teaches that the reconstruction unit is operable to generate data indicating the resources of the very long instruction word processor that correspond to a simulation result of simulating an output dependency instruction according to the update information for the delay instruction and according to the update information for the output dependency instruction that has an output dependency in the same group of instructions as the delay instruction (Page 7, Para 0129; Page 8, Para 0159 and Para 0160; Page 13, Para 0315 and Para 0324; Page 14, Para 0336).

11. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Moller et al.** (U.S. Patent 6,826,522) in view of **Matsumoto et al.** (U.S. Patent Application 2003/0204819), and further in view of **Ussery et al.** (U.S. Patent Application 2001/0025363) and **Miyake et al.** (U.S. Patent 6,681,280).

11.1 As per claim 19, **Moller et al., Matsumoto et al.** and **Ussery et al.** teach simulation apparatus of claim 18. **Moller et al., Matsumoto et al.** and **Ussery et al.** do not expressly teach that the very long instruction word processor to be simulated includes a cancellation unit operable to cancel an execution of an instruction within a plurality of instructions to be simultaneously executed; and the first simulator is operable to simulate the cancellation unit. **Miyake et al.** teaches that the very long instruction word processor to be simulated includes a

cancellation unit operable to cancel an execution of an instruction within a plurality of instructions to be simultaneously executed; and the first simulator is operable to simulate the cancellation unit (CL8, L1-6). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the simulation apparatus of **Matsumoto et al., Moller et al.** and **Ussery et al.** with the simulation apparatus of **Miyake et al.** that included the very long instruction word processor to be simulated including a cancellation unit operable to cancel an execution of an instruction within a plurality of instructions to be simultaneously executed; and the first simulator being operable to simulate the cancellation unit, because that would allow simulating an interrupt control apparatus having break interrupt function for interrupting the execution of a program (CL1, L10-14).

Applicant's Arguments

12. Applicant's arguments filed on December 15, 2006 with respect to claim rejections under 35 USC 112 Second Paragraph and 35 USC 103 (a) have been considered. Claim rejections under 35 USC 112 Second Paragraph are withdrawn in response to claim amendments. Applicant's arguments with respect to claim rejections under 35 USC 103(a) are not persuasive in view of the additional claim amendments made by the applicants.

12.1 As per the Applicant's argument that "Matsumoto does not disclose or suggest the simulation of simultaneous execution of a group of instructions intended to be simultaneously executed; the simulation of Matsumoto is not a simulation of sequential execution of instructions

based on the result of the simultaneous execution of those same instructions intended to be simultaneously executed; Matsumoto does not disclose or suggest the simulation of the first simulation unit or the simulation of the second simulation unit, or any combination thereof; Moller teaches a simulation of a VLIW processor by reordering the timing of the execution of multiple processing stages of instructions; Moller teaches that within a single cycle of the simulation of the VLIW processor the fetch, decode, execute, and condition return operations are simultaneously executed, wherein the fetch, decode, execute, and condition return operations are processing stages of various instructions; referring to cycle 5, the stages which are simultaneously executed are from instruction 5, 4, 3, and 2; any simultaneous execution taught by Moller refers to the simultaneous execution of a set of processing stages that do not come from the same instruction, but rather come from multiple instructions which were not intended to be simultaneously executed; ... the group of instructions intended to be simultaneously executed requires that the same stage (i.e., execution stage) from each instruction Ax, Ay, and Az be simultaneously executed; Moller discloses a single execution of a set of processing stages of an instruction, not intended to be simultaneously executed, by reordering the timing of the multiple processing stages; Moller does not disclose or suggest a simultaneous execution of instructions intended to be simultaneously executed and does not disclose or suggest a sequential execution of the same group of instructions based on the result of the simultaneous execution, or any combination thereof; the combination of Matsumoto in view of Moller fails to disclose or suggest the features of independent claim 1; a person having ordinary skill in the art would not have been motivated to modify the Matsumoto patent in view of the Moller patent in such a

manner as to result in or otherwise render obvious the present invention of claim 1", the examiner has used the **Moller et al.** reference against the amended claims.

The Examiner takes the position that though the specification indicates simultaneous execution of a group of instructions at the same stage of the pipeline execution, the claims do not state that the simultaneous execution implies that all or some of the instructions are required to be at the same stage of the pipeline. Therefore, the Examiner has given wide interpretation to the claims to cover simultaneous execution of different instructions at different stages of the pipeline. The Examiner also takes the position that Moller discloses a simultaneous execution of instructions intended to be simultaneously executed (This is the whole purpose of designing the VLIW processors and simulating them) as shown below in the various art references which talk about simultaneous execution.

Moller et al. teaches a simulation apparatus for simulating a very long instruction word processor (Abstract, L14-16; CL1, L20-22; CL2, L13-14; CL4, L29-37; CL4, L47-49; Fig. 1); the simulation apparatus comprising:

a first simulation unit operable to simulate execution of a group of instructions intended to be simultaneously executed, and to generate a first simulation result (Fig. 4: shows a group of instructions executed on a cycle e.g. cycle 5 with instructions I2-I5; Fig. 8; Fig. 13; CL1, L35-38; CL1, 51-54; CL6, L31-34; CL4, L29-37; CL4, L47-49; Fig. 1; CL6, L37-40; CL8, 21-23; CL8, L55-57) ; and

a second simulation unit operable to simulate, based on the first simulation result generated by the first simulation unit, a sequential execution of the group of instructions on an instruction-by-instruction basis and to generate a second simulation result (CL1, L29-33; Fig. 6: Shows one instruction I1 in one cycle; CL2, L17-30; CL6, L46-51; CL6, L56-62; CL8, L63-65).

ACTION IS FINAL

13. Applicants' extensive amendments necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
February 7, 2007

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

2/9/07